Melvin St.John

  E396M267

Technical Journal

Technical Journal

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# 

# **Week Aug 29 – Sept 4**

## **Goal of the week**

To research the operation of BLDC motors and to familiarize myself with project parameters.

### **General Notes**

The brushless DC motor is a synchronous electric motor that, from a modelling perspective, looks exactly like a DC motor, having a linear relationship between current and torque, voltage, and rpm. It is an electronically controlled commutation system, instead of having a mechanical commutation, which is typical of brushed motors. Additionally, the electromagnets do not move, the permanent magnets rotate, and the armature remains static. This gets around the problem of how to transfer current to a moving armature. To do this, the brush-system/commutator assembly is replaced by an intelligent electronic controller, which performs the same power distribution as a brushed DC motor.

I looked into the Single Event Effects on electronics: <https://www.aerodefensetech.com/component/content/article/adt/features/articles/33364> .

I looked into how other motors are controlled: <https://www.ncbi.nlm.nih.gov/pmc/articles/PMC3231115/>

### Results and Conclusion

There are multiple routes to achieve “control” of this fan motor, but we are not, technically, ‘controlling’ this motor. We are more concerned about monitoring the tach signal. As we are limited to non-programable components, I think we need to consider a simple low pass filter leading into a comparator circuit that would send a signal when the fan isn’t operating within set parameters.

### Next Steps

Given that one of our parameters is to use non-programable components, I am going to look at what the limitations and benefits are of using op-Amps, Mosfets, etc. for our comparator circuit. Which of these best suit our design parameters dealing with temperature, pressure, etc.?

# **Week Sept 4 – Sept 11**

## **Goal of the week**

Familiarize myself with comparator circuits control techniques commonly used by industry and compare the advantages/disadvantages of each with respect to our design parameters.

### **General Notes**

**Op-amps as a ‘comparator’** isn’t always acceptable as their input structure may saturate if over-driven. Input stages may behave in unexpected ways when driven with large differential voltages, or beyond the specified common mode range. The most common issues are speed, the effects of input structures (protection diodes, phase inversion FET amps), output structures are not intended to drive logic, **hysteresis** and stability, and common modes effects.

### Results and Conclusion

Op-amps are still potentially an option for a comparator. The high intrinsic gain of the op-amp and the output saturation effects can be exploited (at a basic level) by setting it up so that it acts like a binary-state decision-making circuit. If the voltage at the + terminal is greater than the voltage at the – terminal, the output goes to high (saturates its max value). If the out goes to low, it could compare the voltages at the two inputs and generate an output based on the relative values.

### Next Steps

Look into dealing with the hysteresis with a feedback loop.

Look into transistor function as a comparator.

# **Week Sept 12 – Sept 18**

## **Goal of the week**

To familiarize myself with techniques to deal with hysteresis within our comparator circuit.

### **General Notes**

The team has, for the moment, decided not to explore transistors in this circuit.

### Results and Conclusion

Diagram, schematic

Description automatically generated please note that I have the Vref and Vin mixed up on this layout.

For an option as a non-inverting hysteresis comparator: Vin is applied to the non-inverting input of the op-amp. R1 and R2 form a voltage divider network across the comparator providing positive feedback that allows part of the output voltage to appear at the non-inverting input along with the Vin via the same resistive divider.

The amount of feedback is determined by the resistive ration of the two resistors. If we use this design the ration would be ½.

The thresholds would be determined as follows:

Diagram

Description automatically generated

### Next Steps

To determine whether it would be better to use a negative feedback rather than positive.

# **Week Sept 19 – Sept 25**

## **Goal of the week**

Compare the negative/positive feedback configurations to ascertain which is more suitable for this application.

### **General Notes**

The basic configuration for the **positive** voltage comparator, also known as a non-inverting comparator circuit, detects when the input signal, VIN is ABOVE or more positive than the reference voltage, VREF producing an output at VOUT which is HIGH as shown.

The reference voltage is connected to the inverting input of the operational amplifier with the input signal connected to the non-inverting input. If the two resistors forming the potential divider network are equal this will produce a fixed reference voltage which is one half that of the supply voltage, that is Vcc/2, while the input voltage is variable from zero to the supply voltage.

When VIN is greater than VREF, the op-amp comparators output will saturate towards the positive supply rail, Vcc. When VIN is less than VREF the op-amp comparators output will change state and saturate at the negative supply rail.

The basic configuration for the **negative** voltage comparator, also known as an inverting comparator circuit, detects when the input signal, VIN is **below** or more negative than the reference voltage, VREF producing an output **at VOUT which is high**.

Diagram, schematic

Description automatically generatedInverting with Hysteresis

When the input signal is less than the reference voltage, VIN < VREF, the output voltage will be HIGH, VOH and equal to the positive saturation voltage. As the output is HIGH and positive, the value of the reference voltage on the non-inverting input will be approximately equal to: +feedback fraction\*V called the Upper Trip Point or UTP.

As the input signal, VIN increases it becomes equal too this upper trip point voltage, VUTP level at the non-inverting input. This causes the comparators output to change state becoming LOW, VOL and equal to the negative saturation voltage as before.

But the difference this time is that a second trip point voltage value is created because a negative voltage now appears at the non-inverting input which is equal to: -feedback fraction\*V as a result of the negative saturation voltage at the output. Then the input signal must now fall below this second voltage level, called the Lower Trip Point or LTP for the voltage comparators output to change or switch back to its original positive state.

So, when the output changes state, the reference voltage at the non-inverting input also changes creating two different reference voltage values and two different switching points. One point being called the Upper Trip Point (UTP), while the other is called the Lower Trip Point (LTP). The difference between these two trip points is the **Hysteresis**.

The amount of hysteresis is determined by the **feedback fraction**. The feedback fraction of the output voltage fed back to the non-inverting input. The advantage of positive feedback is that the resulting comparator Schmitt trigger circuit is immune to erratic triggering caused by noise or slowly changing input signals within the hysteresis band producing a cleaner output signal as the op-amp comparators output is only triggered once.

So, for positive output voltages, VREF = +feedback fraction\*Vcc, but for negative output voltages, VREF = -feedback fraction\*Vcc. The amount of voltage hysteresis will be given as:

Vhyst = Vutp -Vltp

Vhyst = +feedback\*Vcc – (-feedback\*Vcc)

Therefore, Vhyst = 2\*feedback\*Vcc

### Next Steps

Although the team is leaning towards op-amps, I still think it has limitations that would be unsuitable for our project. Op-amps are only optimized for linear operation where the input terminals are at virtually the same voltage levels and its output stage is designed to produce a linear output voltage than is not saturated for long periods of time.

On the other hand, a nonlinear device that utilizes a switching transistor at the output stage rather than an op-amp would allow us to convert an analog input to a digital output signal and use logic gates at the ‘end’ of our circuit. This configuration (at the output) could be configured as a single open collector (drain) transistor switch with the open or closed state rather than actual output voltages.

Further research is needed.

# **Week Sept 26 – Oct 2**

## **Goal of the week**

To gain more knowledge the incorporation of a pull-resistor.

To begin familiarizing myself with LTspice.

### **General Notes**

Information to be reviewed for LTspice:

<https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html> (DOWNLOAD)

<https://www.youtube.com/watch?v=FEGT5dUpdrc> (DC operating point) <https://www.youtube.com/watch?v=eRtO3EZK_Cc> (Temp sweeping)

### Results and Conclusion

Next Steps

As we have narrowed our comparator circuit down (for the most part) to using the LT1638 chip. I need to learn more about how this chip works and why.

I also need to learn more about the open-collector output connection that is used by the tachometer and will be used by our comparator.

I need to investigate the use of a MOSFET to feed our comparator output into ( a switch).

# **Week Oct 3 – Oct 9**

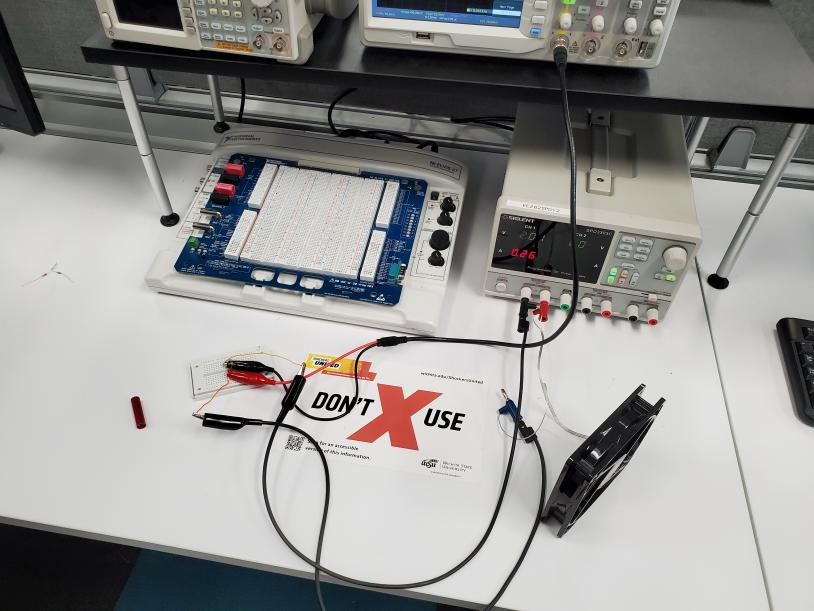
## **Goal of the week**

The main goal of this week is preparation for the midterm presentation.

To learn more about the LT1638 IC and to learn more about the open-collector connection. I also need more information on MOSFET operation. On-going familiarization with LTspice.

### **General Notes**

The goals of the week were sidetracked a bit by getting a test fan. We started testing it to ascertain what the waveform and characteristics looked like.

Open collector notes: it can provide a current sink or a source depending on the connection. MOSFET, unlike a BJT which requires a base current to drive the transistor into saturation, requires a suitable voltage applied to its Gate terminal. The source terminal is connected to ground or the supply rail, while the open-drain terminal is connected to the load. The MOSFET may need a pull-up/pull-down resistor depending on our load requirements.

A picture containing text, clock, gauge

Description automatically generated

The LT1638:



### Results and Conclusion

Next Steps

Look into MOSFET because I didn’t get to this week.

# **Week Oct 10 – Oct 16**

## **Goal of the week**

The main goal of this week is preparation for the assessment test.

### **General Notes**

The majority of this week was spent doing preparation for the ‘assessment’. We did make it to the lab on 15 Oct. to do additional testing on the fan output. We tried to implement a filter after the tach to reduce the noise, but it did not respond as we had anticipated.

### Results and Conclusion

We need to research into how we are supposed to implement the filter on the breadboard to ensure that we did it correctly.

Next Steps

Research further on the filter breadboarding. There is confusion on how to add it with the pull up resister on the tach.

# **Week Oct 17 – Oct 23**

### **General Notes**

Preliminary simulations on the Rc filter.

### Results and Conclusion

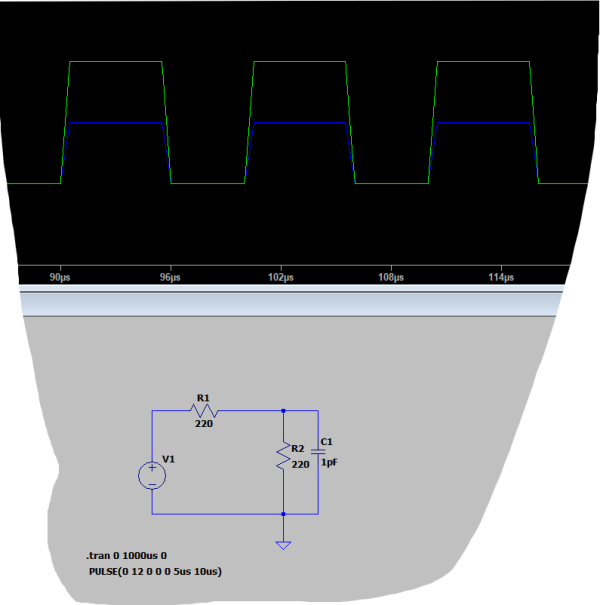
Next Steps

# **Week Oct 24 – Oct 30**

### **General Notes**

Preliminary simulations on the RC filter.

### Results and Conclusion



The above screenshot is of a first run RC filter with and ‘ideal’ source voltage within LtSpice. The voltage has been halved, which I’m assuming is because of ‘over filtering’. I need to adjust values to retain voltage levels and still obtain some filtering effect(i.e., do away with the divider).

A screenshot of a computer

Description automatically generated with medium confidence

Graphical user interface

Description automatically generated

The screenshots above are of the RC filter simulation ran with a signal generated from the test fan provided by Textron.

Graphical user interface

Description automatically generated with medium confidence

A screenshot of a computer

Description automatically generated with medium confidence

Graphical user interface

Description automatically generated

Next Steps

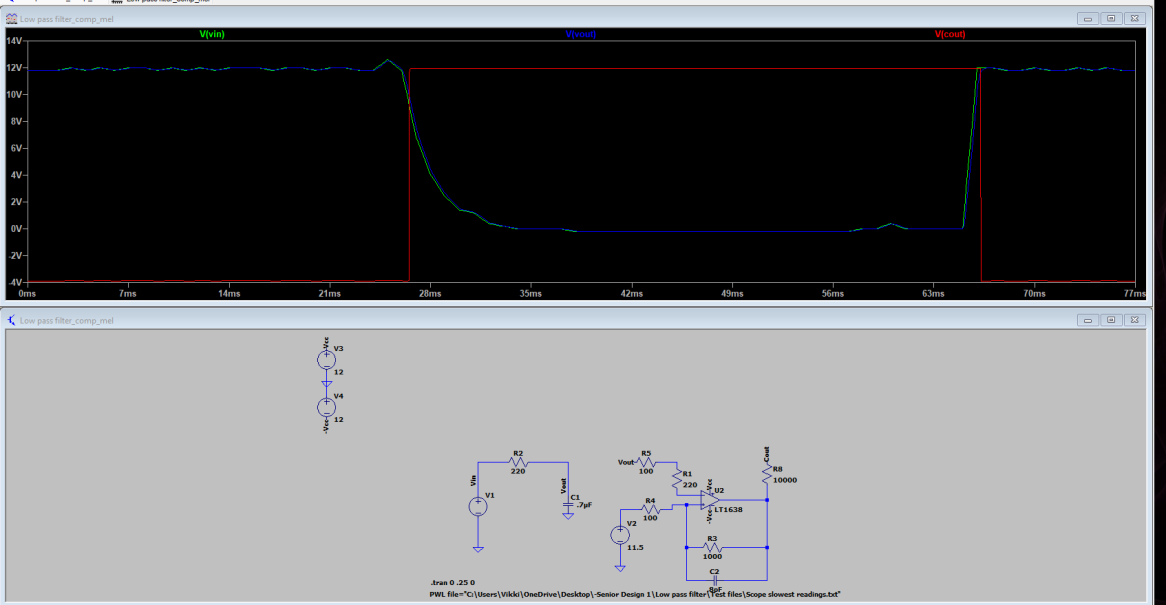
Do a frequency analysis on the filter, set component values to accommodate a 0-1kHz range, and begin to put sections of the general circuit together in LtSpice to ascertain functionality of the design in general.

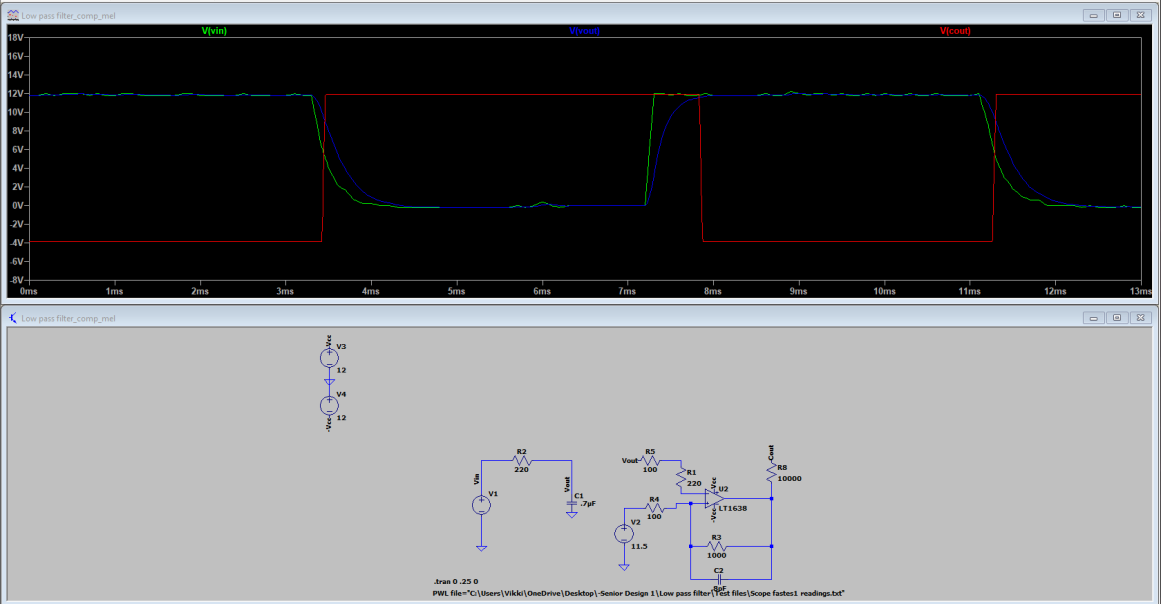
# **Week Oct 31 – Nov 06**

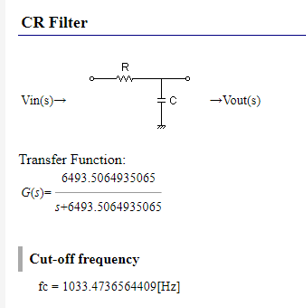
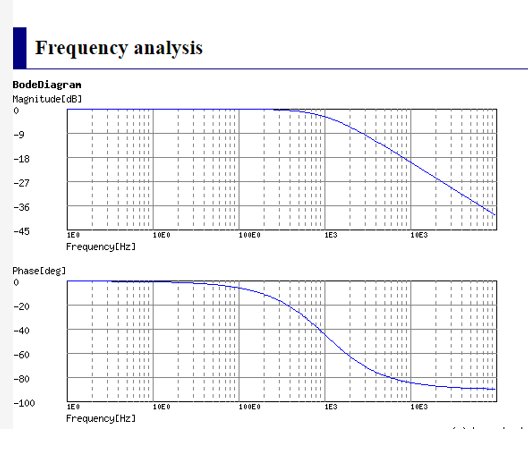
### **General Notes**

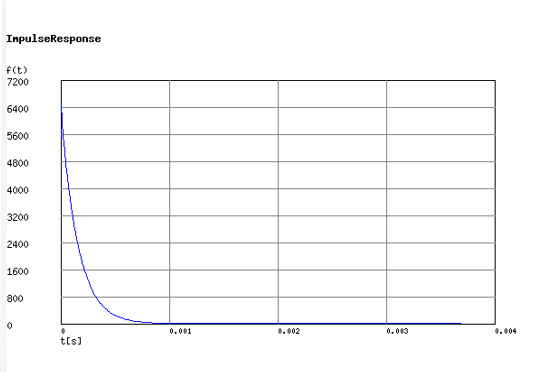
Continued testing on LtSpice of the filter as well as adding in a version of the comparator.

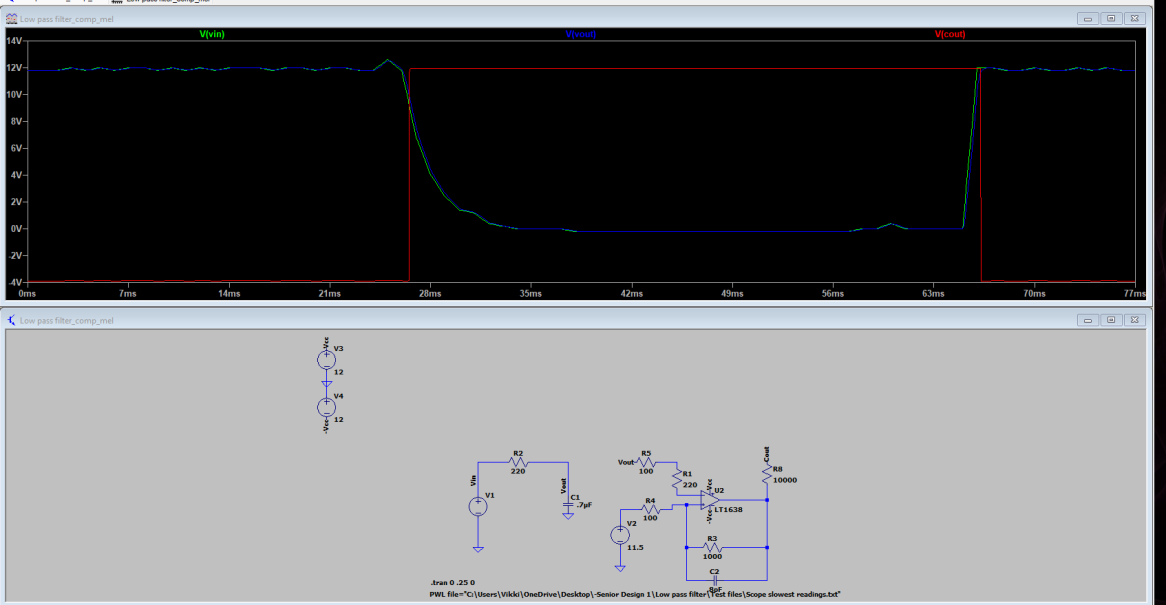
### Results and Conclusion

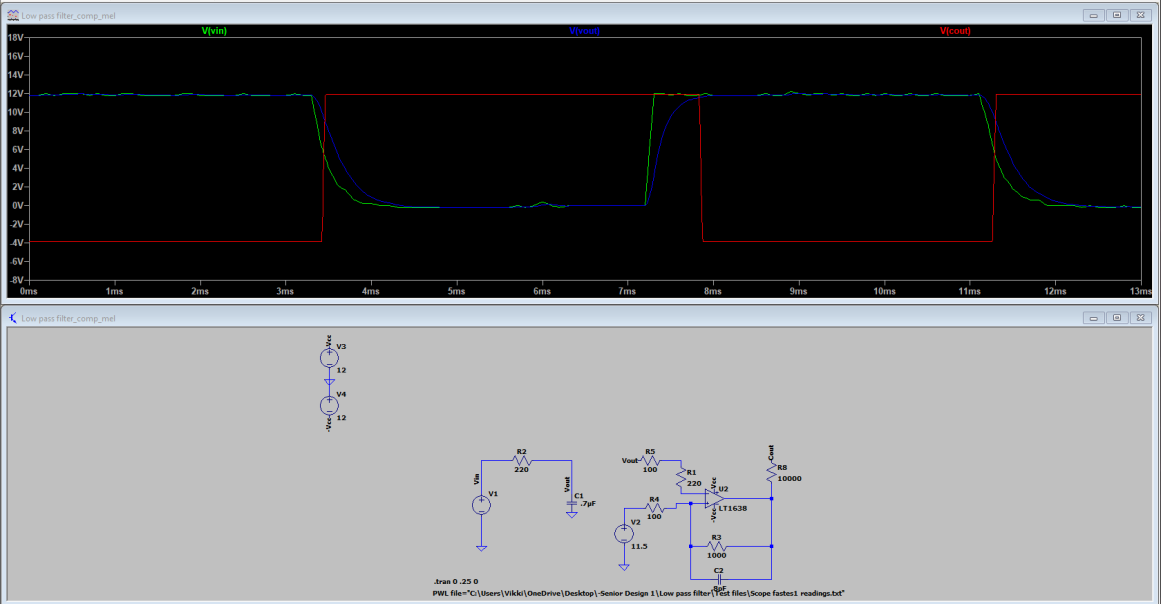










Next Steps

# **Week Nov 07 – Nov 13**

### **General Notes**

### Results and Conclusion

Graphical user interface

Description automatically generated with low confidence Diagram

Description automatically generated

This is a test circuit with and ‘ideal’ square wave 5v input. The rails are powered at 5v and -5v and the reference voltage supplied is 2vdc. We have had problems getting the results that we expected so I reverted back to a ‘ideal’ signal to try and get the waveforms that we were expecting.

Graphical user interface, application, table, Excel

Description automatically generated this is the same circuit with a 4v input.

Graphical user interface

Description automatically generated

Graphical user interface, chart

Description automatically generated

A screenshot of a computer

Description automatically generated with medium confidence

A screenshot of a computer

Description automatically generated with medium confidence this is at 0.5v input.

My concern is that the comparator is not switching even at the lowest input of 0.5 volts. I assume that I need to reevaluate the component values of the resistors for this part of the circuit as well as the reference voltage.

Table

Description automatically generated

I believe I have gotten the comparator to switch now but only at one threshold, it seems.

Graphical user interface

Description automatically generated

Input: 2.84v square wave (green)

Integrator output is the blue

Red is comparator output.

Graphical user interface

Description automatically generated

When input goes to 2.85 volts it switched to high

Next Steps

It is my intent to delve deeper into the comparator portion of the circuit. I need to solve the issue of component values to obtain what I want as an output. At this point, I have a lower trip point but not a upper trip point…Why? Once that issue is resolved, I will get to work on the ability to sink 1 amp continuously.

# **Personal Product Reflection**

**Textron Aviation Cooling Fan Project**

# Introduction

This project is to develop a small circuit board that will monitor the tachometer output of a brushless DC cooling fan, and then control a discrete (ground/open) output to indicate if the cooling fan is functioning as intended. The intent is for the circuit board to be small enough that it can be installed in the aircraft wire bundle with zip ties to support aftermarket and late point definition installations with minimal impact to the aircraft and/or maintenance crew.

# Body

**Interview 1:** Robert Evans

Robert is a research engineer for NIAR in the robotics laboratory and holds a bachelor’s in electrical engineering. He currently works on defence projects through NIAR. Based on his personal work experience, we picked up some interesting, new information based on his perspective. He first mentioned that we should be more specific with the types of circuits we are using (i.e., If we are using a filter, specify that it is a low pass filter). This gives the reader an easier and more direct understanding of the overall circuit. He also mentioned that we should try and find out what kind of wires we will being running this circuit next to, as these wires could create more noise in our signal. While we already have filtering to counter act this, we may have to raise our values on our filters to add a larger cushion for error. He said it would be quite important it to label all components, including cables, inputs/outputs, and the parts on the PCB board itself, as this will make the jobs of the technicians far easier.

One of the most important points he brought up is that many aircraft circuits are “potted”, meaning that the entire PCB board with all the components soldered on is encased in a layer of epoxy. This epoxy could push our design beyond the required size constraints, and he did not seem to think that we would be able to fit that size if we are required to pot our circuit.

Overall, Robert was able to give us good first had knowledge on standards of aircraft parts. We should be more descriptive with our overall circuit by adding more labelling and be specific with our circuit sections. We will need to get into contact with Textron again and see if we can get more information regarding the wires, we’ll be installing this bundle next to, and whether we will be potting this circuit.

**Interview 2:** Dr. John Brewer

Dr. Brewer is a local business owner who holds advanced degrees in Electrical Engineering and a P.H.D. in Physics. He has many years of experience in circuit design and material science. It was his opinion that the circuit, as seen on the block diagram provided, seemed sound in concept. He voiced a concern pertaining to heat dissipation (from the resistors) with such a small package requirement. He also questions whether it would be too large a PCB for our size constraints.

Dr. Brewer is also and experienced pilot and emphasized the need for appropriate labelling both on the PCB and the package. He also stated that, as a pilot, he would want three outputs rather than just the two proposed: one to tell if over rpm; one to tell if operating with range; and one to tell if it was under rpm thresholds. As it pertains to the package, he didn’t believe that 3-D printing (with resin) would be appropriate. He believes that it would be more appropriate to ‘pot’ it. He also stated that we need to used non-flammable materials as well.

Overall, an important take away from this interview was that we need to reconsider our thoughts on the packaging, and research more into what is required by the FAA and DoD regulation for this situation. Secondly, we need to be conscious of our heat generation from the resistors and how it will be dissipated when enclosed within the package.

**Summary**:

The interview process was very educational, and I learned a lot from this experience. As engineers, we should, and must, commit to lifelong learning. The interview process helped me to grow and provided an insight into learning process of a practicing engineer. It also illustrated some blind spots within our original design. Interviewing people to ask them their expectations for a product is very important for the engineering profession. All engineers should ask questions to help them learn who they trying to help, and how they should do it. One thing that I, personally, make a point of doing no matter where I have worked is to talk to everyone regardless of job title. The experience of others is a valuable tool to access when in the real-world work arena. Anyone can contribute insight whether they are a janitor or a PHD.

# **Second Semester Journal Beginning**

# **Week Jan 16 – Jan 22**

### **General Notes**

Generally, reoriented myself with our project with regard to the design, the necessary next steps, and touched base with team members as to their current status.

### Results and Conclusion

We are not where we need to be.

* Need to finish circuit design-finalize component values for voltage divider network (for comparator reference voltage),
* Need to agree on how to get a high impedance output if comparator o/p is **less than** the threshold set
* Need to agree on how to sink 1 amp to ground when o/p is above set thresholds.
* No one on the team has worked on learning Altium, or any other research. Consequently, we still need to :
  + Learn Altium
  + PCB design techniques
* Need to start thermal studies
* Need to research package material requirements with regard to thermal dissipation and Textron requirements.

Main conclusion: WE ARE NOT WHERE WE NEED TO BE AT THIS POINT

# **Week Jan 23 – Jan 29**

### **General Notes**

Worked on the fundamentals of Altium software so as to facilitate our PCB design.

### Results and Conclusion

Text, letter

Description automatically generated

# **Week Jan 30 – Feb 05**

### **General Notes**

Began inputting our design into Altium: transferring schematic, setting up project files, etc.

Continued research into PCB design with Altium.

### Results and Conclusion

I have the bulk of our circuit schematic transferred to Altium.

Still missing:

1. The voltage regulator side
2. The voltage divider for the reference voltage on comparator ( I have it but haven’t added it yet)
3. The high impedance de-assert o/p -high impedance
4. The indication o/p – how to sink one amp to ground (perhaps a MOSFET with a mirror voltage?)

**PCB**

Thermal pads usually have a sticky film on either side and won’t require the steady hand that the paste demands for heat dissipation. All it demands is for you to simply peel the backing off and place it on your CPU. While it might be good to practice using thermal paste, applying a thermal pad will be as simple as applying a sticker.

Heatsinks probably will not be viable since they are difficult to remove thus, making rework (or changing resisters, etc.) problematic.

From: <https://resources.altium.com/p/pcb-temperature>

Mil-grade PCBs, undoubtedly, require materials with higher Tg values. Designers should consider the operating temperature of their mil-grade PCBs while selecting materials. It is always recommended to allocate a minimum **20°C** allowance while choosing the material for your mil-grade PCB. For example: If the operating temperature of a mil-grade PCB is given as 150°C, the material whose Tg value higher than 170°C should be chosen. Materials like **Isola** **FR408HR, DuPont Pyralux, and Nelco N7000-2HT** fall under the high Tg value material category.

If your PCB design requires copper plating of filled vias:

* There shall be no voids that expose filled vias.
* Bumps and depressions on the copper plating of filled vias are acceptable.
* Voids on the copper plating over the filled vias are acceptable.

Other important considerations of mil grade PCB design

* **Rigid PCB base material: GF:**epoxy resin, flame resistant, woven E-glass
* **Maximum panel size:** 18’’ x 24’’
* **Maximum number of layers:**20
* **Maximum board thickness:**100 mils
* **Minimum hole size:** 0.007″ (7 mils) laser-ablated plated hole size before plating, 0.01”(10 mils) drilled the plated-through hole before plating
* **Aspect ratio:**6: 1 for microvias; 10:1 for through-holes
* **Minimum conductor width/space:** 0.004”/0.004”
* [**Surface finish**](https://www.protoexpress.com/blog/surface-finish-pcb-manufacturing/)**:** HASL and ENIG
* **IPC standard**: Class 3 is the highest IPC standard. Mil grade PCBs should be designed and manufactured based on the standards applicable to class 3 PCBs. These standards include laminate selection, plating thickness, material qualifications, manufacturing processes, and inspection.

# **Week Feb 06 – Feb 12**

### **General Notes**

Research more about Altium

Finalized voltage divider circuit for comparator reference voltage (will discuss with the team tomorrow)

Need to discuss using a 10k pullup resister for when the o/p of comparator is less then threshold (high impedance de-assert o/p -high impedance)

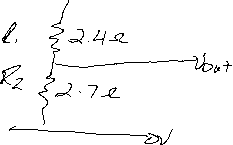
Research into constant current sinks.

### Results and Conclusion

Altium

<https://www.altium.com/documentation/altium-designer/from-idea-to-manufacture-driving-a-pcb-design-through-altium-designer>

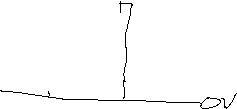
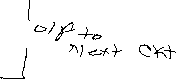
Notes:



We need slightly less than 2.5v for our comparator reference voltage. This gives us 2.35.

Constant current sink with MOSFET

perhaps a current mirror set up?



the sink current could then be limited to what MOSFET 1 provides; current in 2 will be same if two M’s are identical.



I think we will need to find a M with a V-th on the low side, preferable below one volt.

**PCB Update:**

minimum clearances:

* Trace to Trace Clearance: 7 mil
* Trace to Pad Clearance: 7 mil
* Pad to Pad Clearance: 7 mil
* Hole to Hole Clearance: 10 mil
* Minimum Trace Width: 7 mil
* Component Clearance: 1 mil

 minimum component clearance assumes the footprint for the part includes the worst case tolerance stackup for the size of the part.

4 layer board

Further PCB notes:

 FR-4 substrate material does not work for high-frequency circuits. Furthermore, the dielectric constant of FR-4 does not remain constant with changes in temperature. If the temperature range for the application increases, the variations become more significant and cause the impedance to change. In addition, the variations in dielectric constant also affect the capability to achieve and maintain a flat response as frequencies increase.

Calendar

Description automatically generated with medium confidence



Taken from: <https://resources.altium.com/p/pcb-material-selection-how-substrate-properties-impact-pcb-performance>

# **Week Feb 13 – Feb 26**

### **General Notes**

* We decided to use our “half-out” o/p from the voltage regulator as the source for our reference voltage as this would reduce our component number by two resistors.
* A decision was made in consultation with Clinton that there was a need for lightning protection on the input of the circuit (from fan). We will probably use a combination of 1 resistor leading to two diodes (one to ground, one to Vcc).
* Clinton thinks we have a working circuit now. We just need to adjust a few value to accommodate the use of the half-out for the reference and incorporate the lightning protection at the input.
* I continue with the Altium software…will incorporate the changes this week.
  + I am also researching the procedure to make libraries for the footprints.
  + Setting up the layer stack.
    - We are doing a 4-layer board.
  + And, how to make a two-sided board in case there is need.

### Results and Conclusion

I have referenced the following videos/sites in learning about footprints and layer stacks:

1. <https://www.youtube.com/watch?v=PqFtSpAXB9Q>
2. <https://www.youtube.com/watch?v=wxYbIGV9_CY>
3. <https://www.youtube.com/watch?v=vNJxPSeGDWk>
4. <https://app.ultralibrarian.com/Account/Register>

The **first** video:

3:47-9:40 creating/drawing a schematic symbol

45:15-47:50 How to download and import footprint

47:51-50:00 Importing schematic into PCB

52:48-53:50 PCB and changing board shape

53:50- 55:38 PCB stack up

The **second** video references how to create a resistor footprint from scratch from: 0:00-6:09

6:10-14:20 Importing 3-d models

48:18-52:43 Assigning footprints to symbols

The **third** video:

6:47-9:15 Material selection for 4-layer boards

The **fourth** video:

This is a site to find cad files for 3-d models and footprints

The majority of this time period was spent studying the reference materials and trying to put it to use within the project Altium file.

# **Week Feb 27 – Mar 12**

### **General Notes**

### Results and Conclusion

# **Week Mar 13 – Mar 26**

### **General Notes**

### Results and Conclusion

# **Week Mar 27 – Apr 09**

### **General Notes**

### Results and Conclusion

# **Week Apr 10– Apr 23**

### **General Notes**

### Results and Conclusion

# **Week Apr 24– Apr 30**

### **General Notes**

### Results and Conclusion